SV - 455

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Seat No.	

T.E. (ETC) (Semester - VI) (Revised) Examination, May - 2018

VLSI Design

Sub. Code : 66917

Day and Date : Saturday, 05 - 05 - 2018 **Total Marks : 100**

Time : 02.30 p.m. to 05.30 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Assume suitable data whenever necessary.**
3) **Neat diagrams must be drawn whenever necessary.**
4) **Figures to the right indicate full marks.**

Q1) Solve any three. **[18]**

a) Explain concurrent statements in VHDL with example.

b) Briefly elaborate with suitable example, the significance of 'configuration' in VHDL.

c) Explain briefly the different levels of abstraction.

d) Explain positive edge D type flip-flop. Write a VHDL code for same using 'wait' statement.

Q2) Solve any two. **[16]**

a) Which are the different types of 'Operators' that operator on signals, variables and constants in VHDL? Summarize all types and with suitable examples elaborate 'Shift' kind of operators.

b) With the help of neat block diagram explain VLSI system design flow.

c) Explain 4 bit comparator? Write VHDL code for the same.

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Q3) Solve any two : **[16]**

a) Write a VHDL code for 4-bit up counter with enable and Asynchronous reset.

b) Explain 'Transport' and 'Inertial' delay with suitable examples and respective timing diagrams.

c) Using 2 to 4 decoder draw 4 to 16 decoder? Write VHDL code for same.

Q4) Solve any three : **[18]**

a) Explain loop statements used in Verilog with example.

b) Explain 3:8 decoder design using Verilog.

c) Explain following with reference to MOSFET

i) Velocity Saturation

ii) Mobility degradation.

d) Explain Hot Electron effect.

Q5) Solve any two : **[16]**

a) Explain dynamic power dissipation in CMOS circuit.

b) Draw and explain architectural block diagram of XC9572 CPLD.

c) Which are the different fault models used while testing combinational logic circuits? Explain any one in detail.

Q6) Solve any two : **[16]**

a) Explain briefly boundary scan methodology used for testing circuit boards with many ICs.

b) Draw and explain general architectural block diagram of Spartan III family FPGA.

c) Explain how the voltage transfer characteristic for the CMOS inverter can be obtained.