SL - 782

Seat No.	

Total No. of Pages : 2

T.E (Electronics and Telecommunication) (Part - III) (Semester - VI) Examination, April - 2017
VLSI DESIGN (Revised)
Sub. Code : 66917

Day and Date : Friday, 28 - 04 - 2017 **Total Marks : 100**

Time : 02.00 p.m to 05.00 p.m.

Instructions:
1) **All main questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if necessary.**
4) **Draw diagrams and Truth Tables wherever necessary.**

Q1) Attempt any three of the following : **[3 × 6 = 18]**

a) Describe different levels of abstraction in VHDL.

b) Write VHDL code for 4:1 Multiplexer using any concurrent statement.

c) Write the meaning of 'Identifiers' used in VHDL. With suitable examples write the various rules to look at before choosing any identifier.

d) Explain any three types of operators in VHDL with example for each.

e) Explain Inertial and Transport delays in VHDL.

Q2) Attempt any two of the following : **[2 × 8 = 16]**

a) Draw and explain VLSI Design Flow.

b) What is configuration in VHDL? Explain with suitable example.

c) Write Circuit diagram and VHDLcode for 4-bit Ripple Carry Adder using Full Adder as a component. Make use of Generate statement.

Q3) Answer any two of the following : **[2 × 8 = 16]**

a) Design a Mealy FSM to detect 1001 overlapping sequence. Write a VHDL code for the same.

b) Write truth table, entity diagram and VHDL code for synchronous reset D flip-flop using wait statement.

c) Explain attributes in VHDL with example.

P.T.O.

Q4) Attempt any three of the following : **[3 × 6 = 18]**

a) Briefly explain about Assignment and Control statements in Verilog with examples.

b) Write Verilog code for

i) 4:2 Encoder

ii) 1:4 De-multiplexer

c) Draw physical structure of MOS Transistor(MOSFET). Explain the V-I characteristics of the same.

d) Write a Verilog code for 4 bit counter which counts only even numbers. Also provide Reset input for the counter.

Q.5 Answer any two of the following: **[2 × 8 = 16]**

a) Derive the expression for Drain current I_D of MOSFET in

i) Linear/Resistive region

ii) Saturation region

b) Neatly draw and explain functional block diagram of XC9500 macrocell

c) Draw the neat circuit diagram for Configurable Logic Block (CLB) used in Spartan 3E series of Xilinx make FPGA. Explain functionality of each component used inside.

Q.6 Attempt any two of the following: **[2 × 8 = 16]**

a) Explain the following methodologies for testing combinational circuits. Take an example for each.

i) Stuck-at-Fault Models

ii) Path sensitization

b) Briefly write about Built-In-Self-Test used for testing digital ICs. With a neat diagram explain of 4-bit BILBO Register.

c) Write a VHDL/Verilog code for 4-bit serial in serial out shift register using single D flip flop as a component.

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