SF-528

Seat No.	

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T.E. (Electronics & Telecommunication) (Part-III) (Semester-VI) (Revised) Examination, November - 2017

VLSI DESIGN

Sub. Code : 66917

Day and Date : Thursday, 02-11-2017 **Total Marks : 100**

Time : 2.30 p.m. to 5.30 p.m.

Instructions :
1) **All main questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if necessary.**
4) **Draw diagrams and Truth Tables wherever necessary.**

Q1) Attempt any three of the following: **[3×6=18]**

a) What is the need of HDL? Explain the capabilities of VHDL.

b) Write VHDL code for 1:4 De-multiplexer.

c) Write a short note on - Libraries in VHDL.

d) Explain the following VHDL statements with syntax and example

i) Process ii) With-Select

e) Write VHDL code for D Flip-flop with asynchronous reset.

Q2) Attempt any two of the following: **[2×8=16]**

a) Draw an explain VLSI Design Flow.

b) What is a package in VHDL? Write its syntax and explain with suitable example.

c) Write VHDL code for

i) Parity Generator ii) Parity Checker

Q3) Attempt any two of the following: **[2×8=16]**

a) What are the different forms of wait statement? Explain with example.

b) Design a Mealy machine for sequence detector to detect overlapping sequence 1010. Write VHDL code for the same.

c) Explain attributes in VHDL with example.

P.T.O.

Q4) Attempt any three of the following: **[3×6=18]**

a) Briefly explain about Data Types in Verilog with examples.

b) Write Verilog code for

i) Full Adder ii) Binary to Gray code converter

c) Draw physical structure of MOS Transistor (MOSFET). Explain the V-I characteristics of the same.

d) Write a Verilog code for 4 bit counter with Reset and Enable inputs.

Q5) Answer any two of the following: **[2×8=16]**

a) Derive the expression for Drain current I_D of MOSFET in

i) Linear/resistive region ii) Saturation region

b) Draw and explain in detail the product term allocator in a macrocell within Function Block of XC9500 series.

c) Draw and expalin in detail the basic block diagram of Spartan 3E family FPGA.

Q6) Attempt any two of the following: **[2×8=16]**

a) Explain the following methodologies for testing combinational circuits. Take an example for each.

i) Stuck-at-Fault Models ii) Path sensitization

b) With the help of typical boundary scan cell diagram and basic boundary scan architecture explain the concept of boundary scan testing.

c) Write a VHDL/Verilog code for 4-bit Ripple Carry Adder, using Full adder as component.