| Seat No. | |

T.E. (Electronics & Telecommunication) (Semester - VI) (Revised) Examination, April - 2016
VLSI DESIGN

Sub. Code : 66917

Day and Date : Monday, 18 - 04 - 2016.

Time : 03.00 p.m. to 06.00 p.m.

Total Marks : 100

Instructions :
1) All questions are compulsory.
2) Assume suitable data wherever necessary.
3) Neat diagrams must be drawn wherever necessary.
4) Figures to the right indicate full marks.

Q1) Solve any three : [18]
   a) Briefly write about various features and capabilities of VHDL language.
   b) Which are different types of 'Operators' that operate on signals variables and constants in VHDL? Summarize all types and with suitable examples. Elaborate 'Logical' operators.
   c) Write VHDL code for Mod-6 counter.
   d) Write VHDL code for 4:1 multiplexer.

Q2) Solve any two : [16]
   a) Which are the different types of 'Attributes' to which VHDL support? Elaborate 'Signal' type of attributes with proper syntax and its function.
   b) Draw VLSI system design flow diagram and briefly explain each block.
   c) Write a VHDL code for 'D' flip-flop with asynchronous set and reset inputs. Draw entity diagram also.

Q3) Solve any two : [16]
   a) Explain sequential statements n VHDL with example.
   b) Draw a state diagram for a sequence detector '1011' which is realized as a Mealy machine. Write VHDL code for same.
   c) What is meant by 'Package' in VHDL? With the help of proper syntax briefly write package body and package declaration.

P.T.O.

Q4) Solve any three : [18]

- a) Explain control statements used in Verilog with example.
- b) Explain Half Adder design using Verilog.
- c) Explain Hot Electron effect.
- d) Explain operators used in Verilog.

Q5) Solve any two : [16]

- a) Neatly draw and explain functional block diagram of XC 9572 macrocell.
- b) Explain briefly the concept of fault detection using path sensitization technique used in combinational logic circuit testing.
- c) With the help of typical boundary scan cell diagram and basic boundary scan architecture explain the concept of boundary scan testing.

Q6) Solve any two : [16]

- a) Briefly write about Built - In - Test used for testing digital IC's.
- b) Define Power Delay Product in CMOS? Explain in detail.
- c) Draw and explain general architectural block diagram of Spartan III family FPGA.

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