Seat No.

T.E.(Electronics and TelecommunicationEngineering) (Semester -VI)(Old)Examination, April - 2016 VLSI Design Sub. Code: 45694

Day and Date : Thursday, 21 - 04 - 2016   **Total Marks :100**
Time :03.00 p.m. to 6.00 p.m.

Instructions :   1)   All questions are compulsory.
                   2)   Numbers to the right indicates full marks.
                   3)   Assume suitable data wherever necessary.
                              SECTION-I

Q1) Solve any three:-   **[18]**

a)   Which are the different types of 'Operators' that operate on signals,variables and constants in VHDL? Summarize all types and with suitable examples,elaborate'Logical' operators.

b)   Write a VHDL code for 3:8 decoder using 'Case' statement.

c)   With suitable examples of each class, briefly write about various classes of data types used in VHDL programming.

d)   Differentiate MOORE and MELAY machines with suitable examples.

Q2) Solve any two:-   **[16]**

a)   With neat and suitable block diagram, briefly explain VLSI design flow.

b)   Write a VHDL code for 4:1, 8 bit wide multiplexer using behavioral, and data flow type of modeling.

c)   What is meant by 'clock skew' and 'clock jitter'? Briefly write about these concepts with suitable examples.

P.T.O.

Q3) Solve any two: [16]

a) Explain briefly the different levels of abstraction.

b) Write a VHDL code for 4 bit Johnson counter using structural type of modeling.

c) Write a VHDL code for BCD to 7-segment(common anode type)decoder.

SECTION-II

Q4) Solve any three: [18]

a) Which are the different types of 'Attributes' to which VHDL supports? Elaborate 'Array' type of attributes with proper syntax and its function.

b) What is the role of simulators in VHDL code testing? Elaborate cycle based simulator with suitable example.

c) Explain'inertial' and 'transport' delay used in VHDL programming with suitable examples. Draw the respective timing diagrams also.

d) Write a VHDL code for 'D' flip flop with 2-to-1 multiplexer at the 'D' input using WAIT statement.

Q5) Solve any two: [16]

a) Draw and explain complete block diagram of data path section of general purpose microprocessor EC-2.

b) With the help of neat sketch diagram explain XC9572 input/output block which interfaces internal logic with I/O pins.

c) Explain briefly with suitable example Built In Self Testing(BIST) technique used in testing digital ICs.

Q6) Solve any two:-   [16]

a) Briefly write about s-a-1(stuck-at-1) and s-a-0(stuck-at-0)model faults with suitable examples used while testing combinational logic.

b) Explain the concept of look-up table used in CLB of Spartan-II FPGA.Draw necessary sketches of LUT and CLB.

c) Draw the complete block diagram of EC-2 general purpose microprocessor. Briefly write about the various instructions derived for the same.

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